

Figure 1
100

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Figure 2

170

Scan Logic

Test Enable Circuitry

Boundary-Scan Register

I/O Loop Back
Pattern Generator

Capture and Check Logic

Boundary-Scan Register

I/O Loop Back Compare
Circuitry

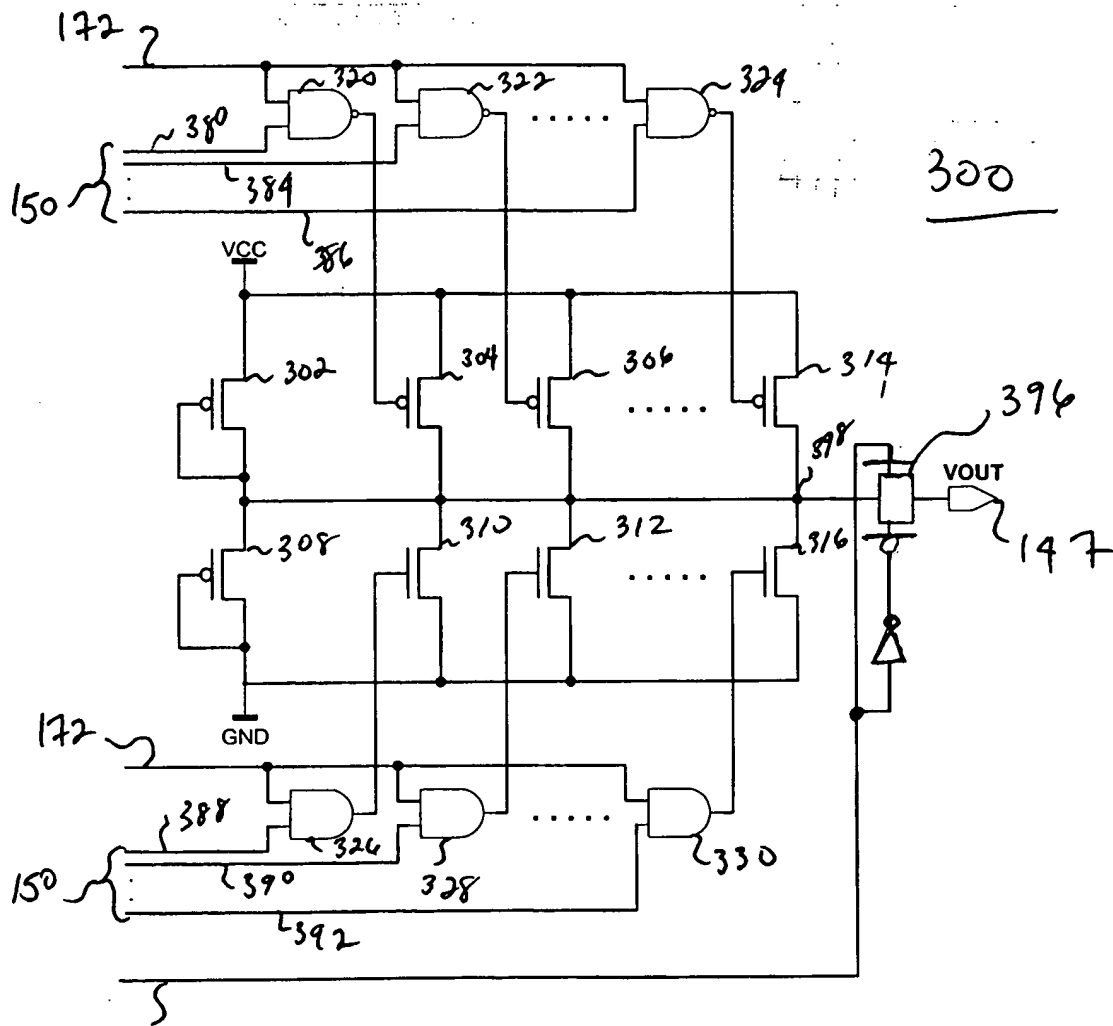
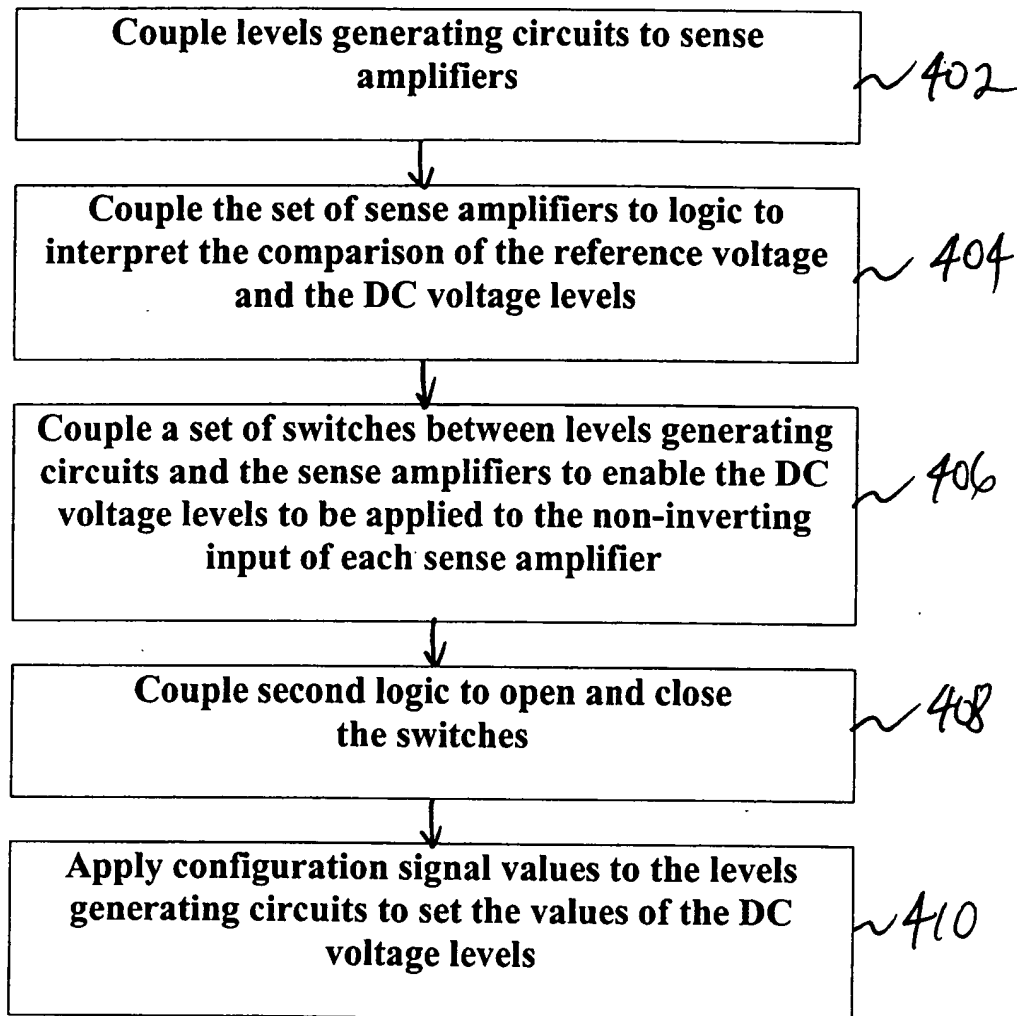


Figure 3

Figure 4
400



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